SIS1100/3100
and SIS3820
Xilinx programming

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Version: 1.40 as of 04.11.05

Revision Table:

Revision	Date	Modification
0.1	12.12.01	Generation
1.0	11.04.02	First official release, change to iMPACT
1.10	12.04.02	change to WebPACK42wp00, add SIS9200 section
1.20	16.04.03	SIS3100 with shortened JTAG chain for later XC2S200 FPGAs
1.30	23.06.2003	SIS3820 added
1.40	04.11.05	iMPACT download

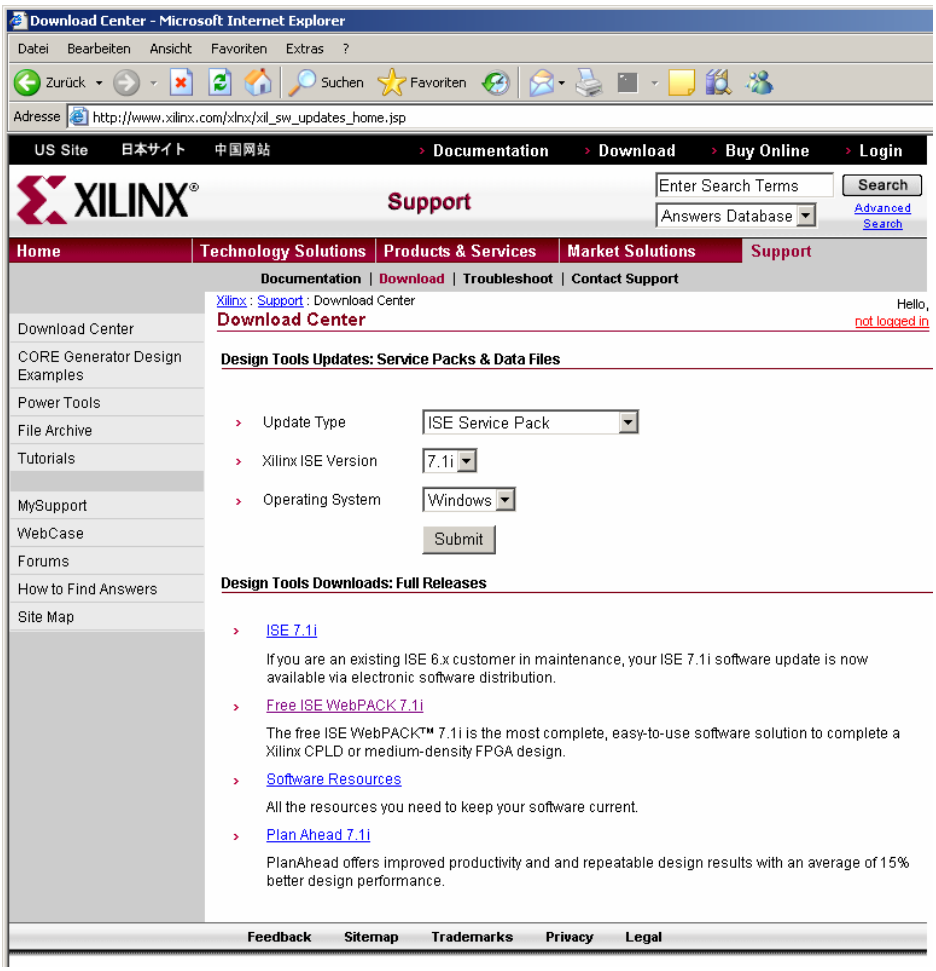
1 Table of contents

2 Introduction

This document describes the firmware upgrade procedure of the SIS1100, SIS3100 and SIS3820 cards via the JTAG port. The procedure was tested with a laptop under Windows 2000 and a Xilinx parallel port JTAG programming cable (i.e. HW-JTAG-PC).

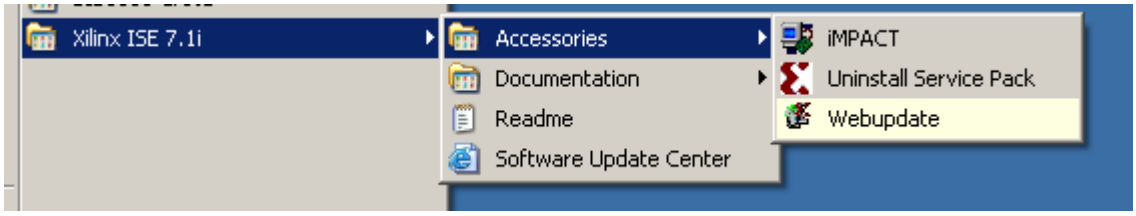
3 Installation of iMPACT software

The iMPACT software is part of the ISE WebPACK, which can be downloaded from www.xilinx.com after creating/login onto a Xilinx account. You will find the free ISE WebPACK x.yi in the support download area as illustrated (for 7.1.i) below.



can be found on the

After installation you should have iMPACT on your PC as shown below. The iMPACT program is used to install the firmware over JTAG.

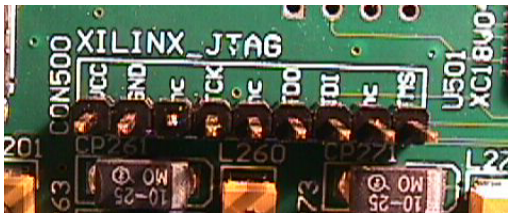


3.1 JTAG connection

Connect the JTAG cable to the parallel port and to the SIS3100 or SIS1100 (both modules have different pinout for the JTAG port for historic reasons, they are listed below).
Start the software by double clicking the Icon on the desktop.

3.2 SIS3100

A photograph with the JTAG connector of the SIS3100 is shown below.

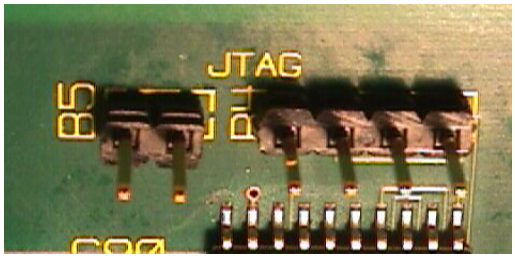


Pinning of :SIS3100 JTAG connector (XILINX_JTAG):

Pin	Pin designator
1	VCC
2	GND
3	nc
4	TCK
5	nc
6	TDO
7	TDI
8	nc
9	TMS

3.3 SIS1100

A photograph with the JTAG connector of the SIS1100 is shown below.



Pinning of :SIS1100 JTAG connector (B5/B4):

B5:

Pin	Function
1	VCC
2	GND

B4:

Pin	Function
1	TCK
2	TDO
3	TDI
4	TMS

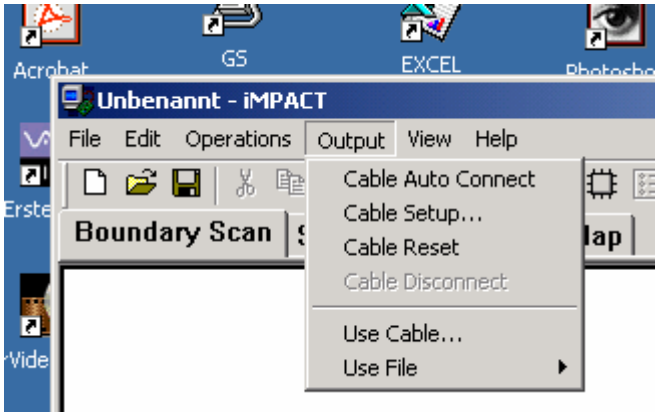
4 SIS3100 firmware upgrade

The SI3100 firmware upgrade is explained in a little more detail, the procedure for the SIS1100 is similar and should be straightforward once you are done with the procedure for the SIS3100.

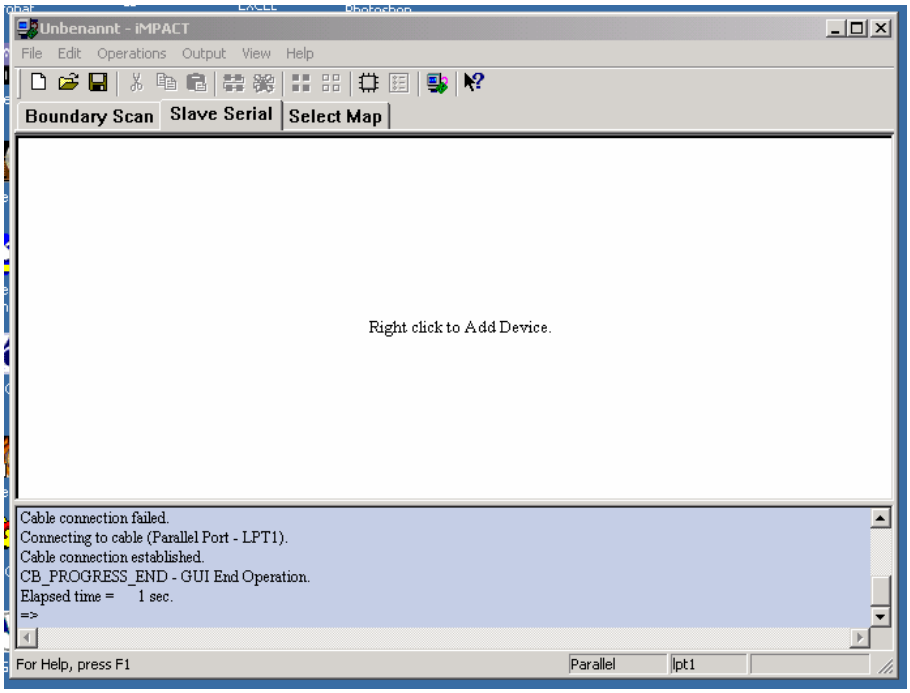
4.1 Establish Cable Connection

First you will have to establish a connection to your computers port (LPT1 in the example below).

At first startup you may have to select a connection, you may want to use Cable Auto Connect to do so.

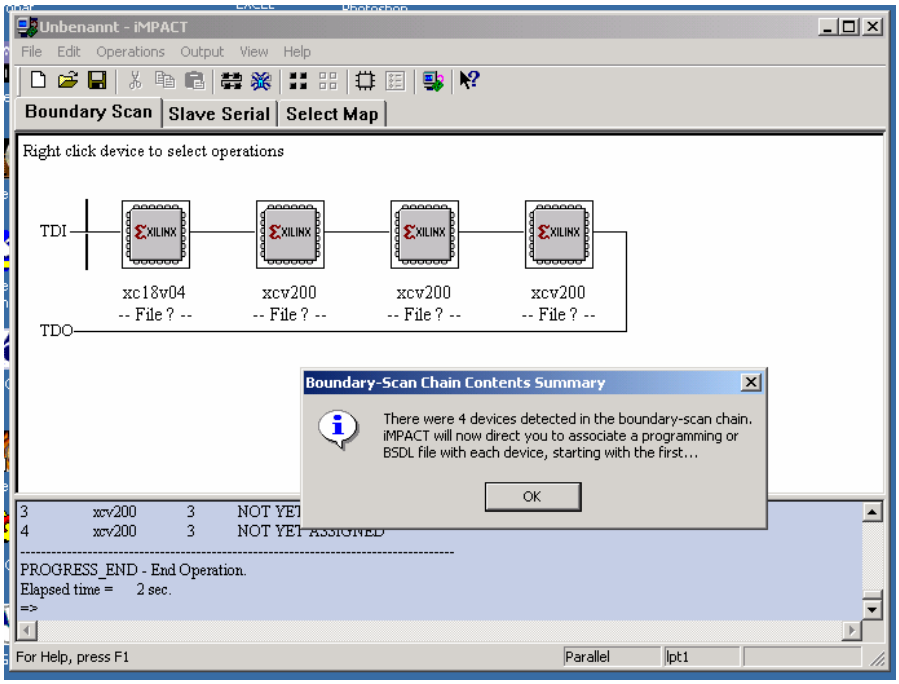


Once you have a proper connection established your screen will look like below.



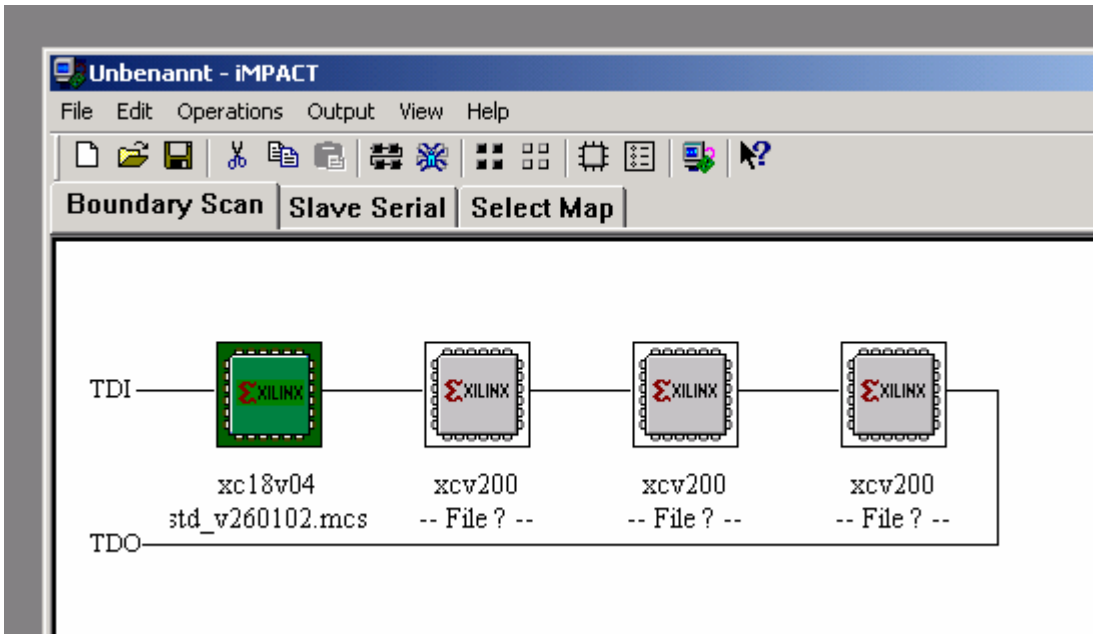
4.2 Initialize chain

In this step the hardware will try to detect/initialize the JTAG devices in the chain. In the case of the SIS3100 one serial PROM (XC18V04) and 3 Spartan 2 FPGAs (reported as XCV200 Virtex FPGAs) have to be detected (if a SIS9200 DSP is installed and the JTAG chain is routed over the DSP you may see additional devices, refer to section 5 also).
Refer to section shortened JTAG chain on SIS3100 modules that exhibit problems in this step after complete firmware loss.
Note: the SIS3100 will have to be under VME power for programming



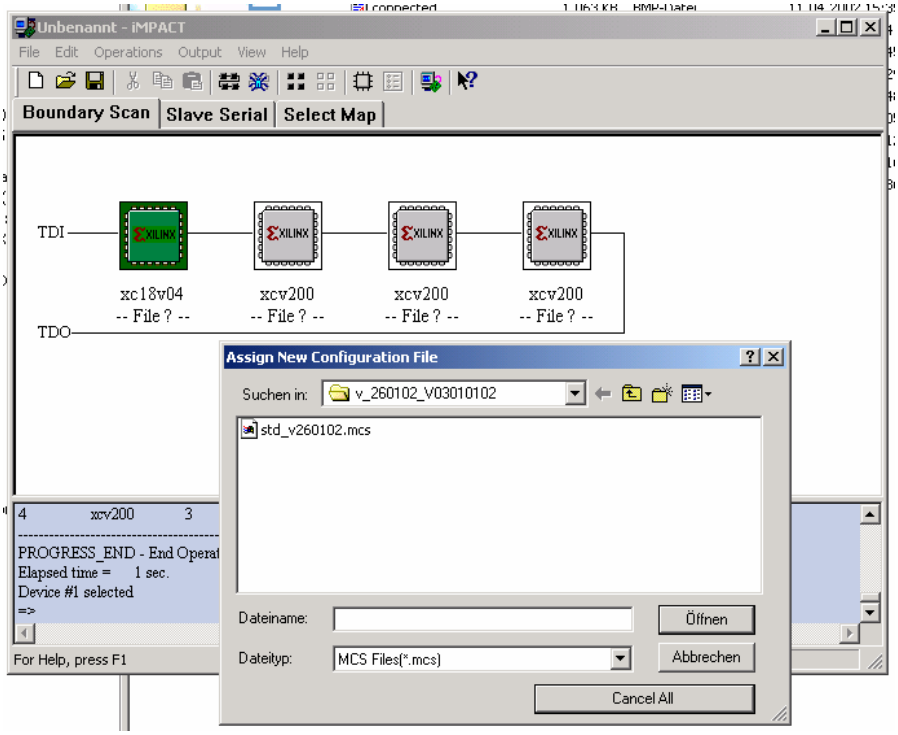
4.3 Select device

The only device that will be programmed is the XC18V04 serial PROM. Select the device by double clicking on it.



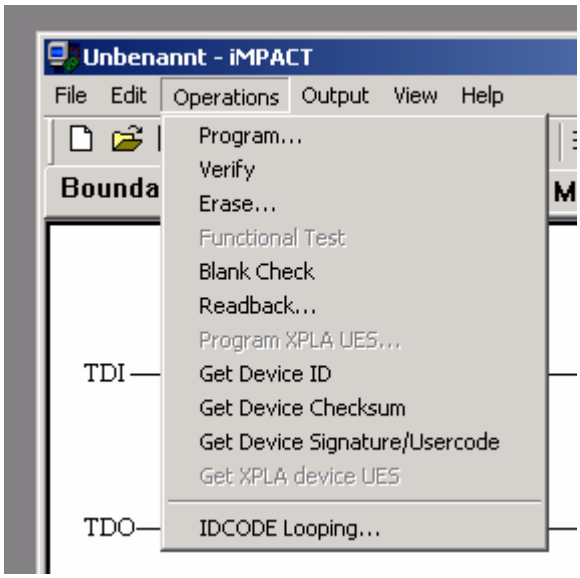
4.4 Select programming file

Select the programming file with the File pulldown and use cancel all afterwards, as the FPGAs will not need to be programmed..

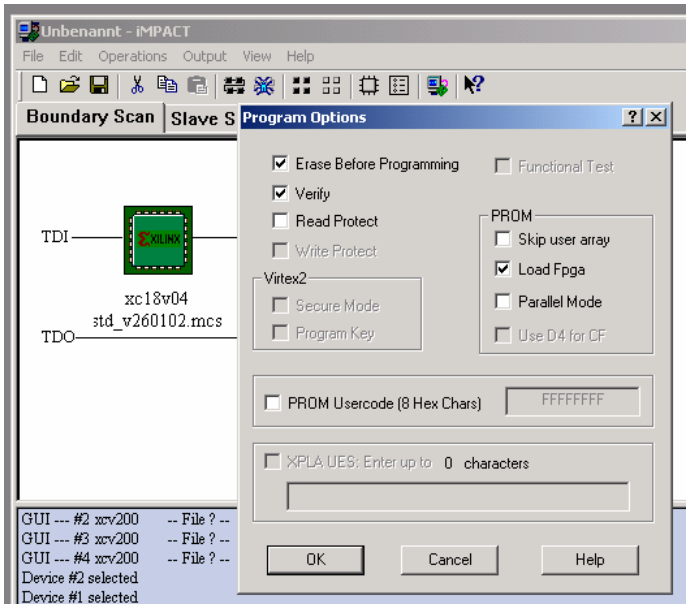


4.5 Program

Select Program from the Operations pulldown.

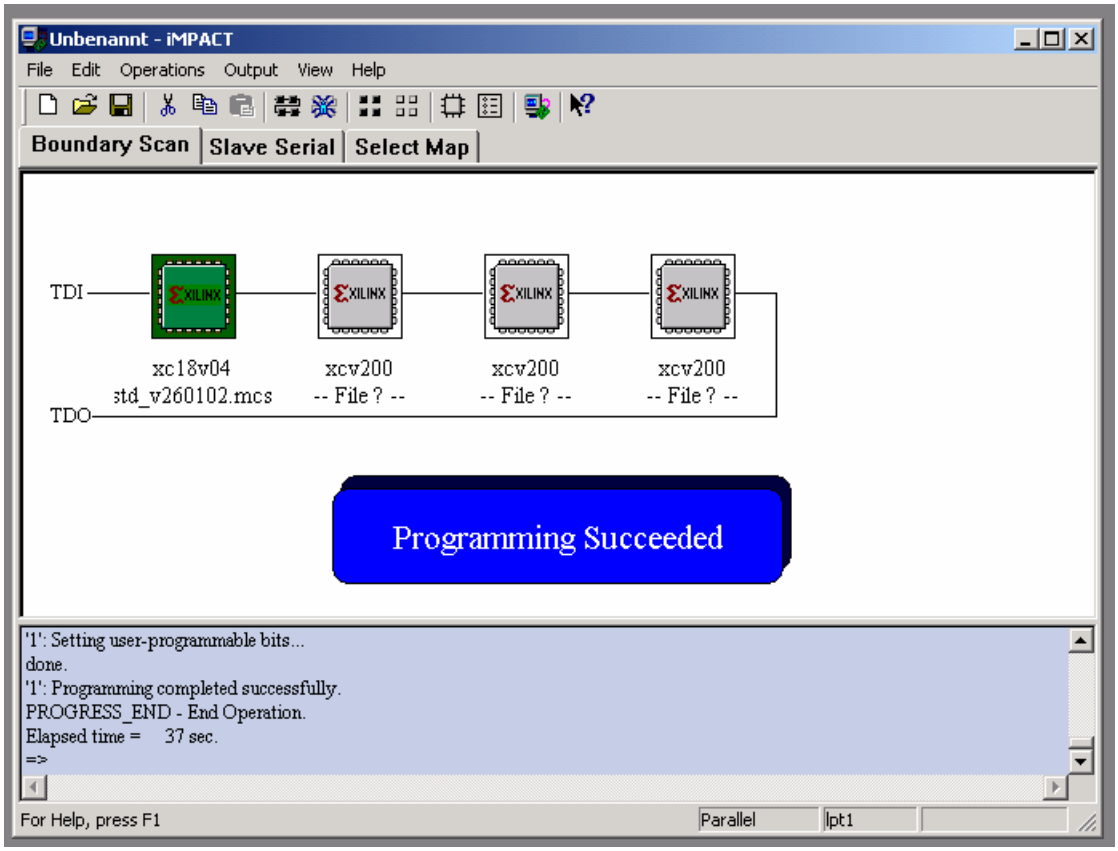

Unbenannt - iMPACT
File
Edit
Operations
Output
View
Help
Program...
Verify
Erase...
Functional Test
Blank Check
Readback...
Program XPLA UES...
Get Device ID
Get Device Checksum
Get Device Signature/Usercode
Get XPLA device UES
IDCODE Looping...
TDI
TDO

We will want to erase, program, verify and Load FPGA (a power cycle will be required after the firmware has been rolled in anyway).



4.6 Succeeded/completed

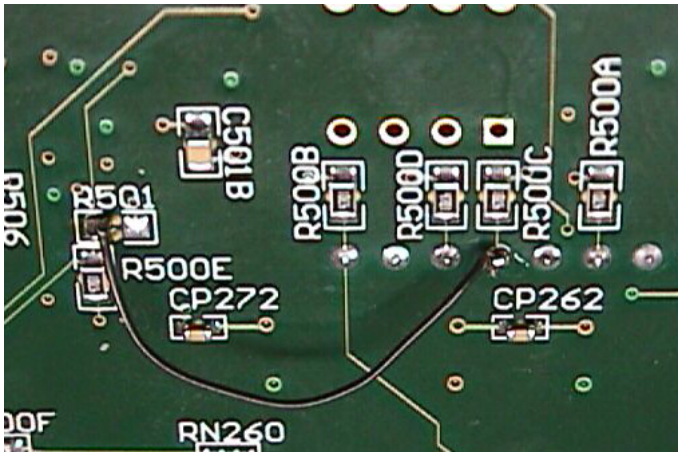
Upon successful completion the programming succeeded message will pop up for a while.



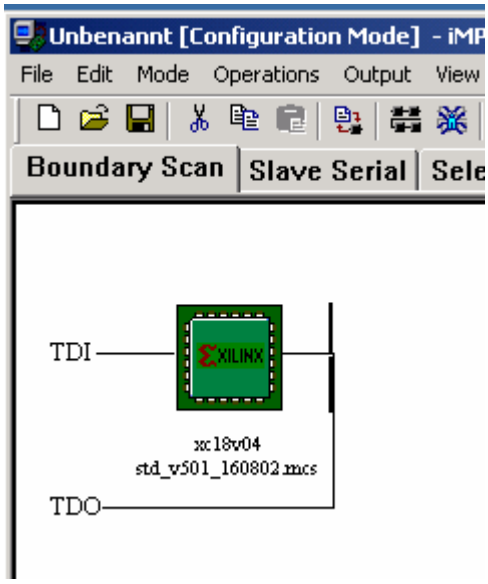
4.7 shortened JTAG chain

You may have to shorten the JTAG chain of the SIS3100 after a complete loss of firmware or the download of wrong firmware. This is done by connecting the left pin of SMD resistor pad R501

to the TDO signal (as shown on the photograph below) and opening jumper J_DSP and unplug a possibly installed SIS9200.



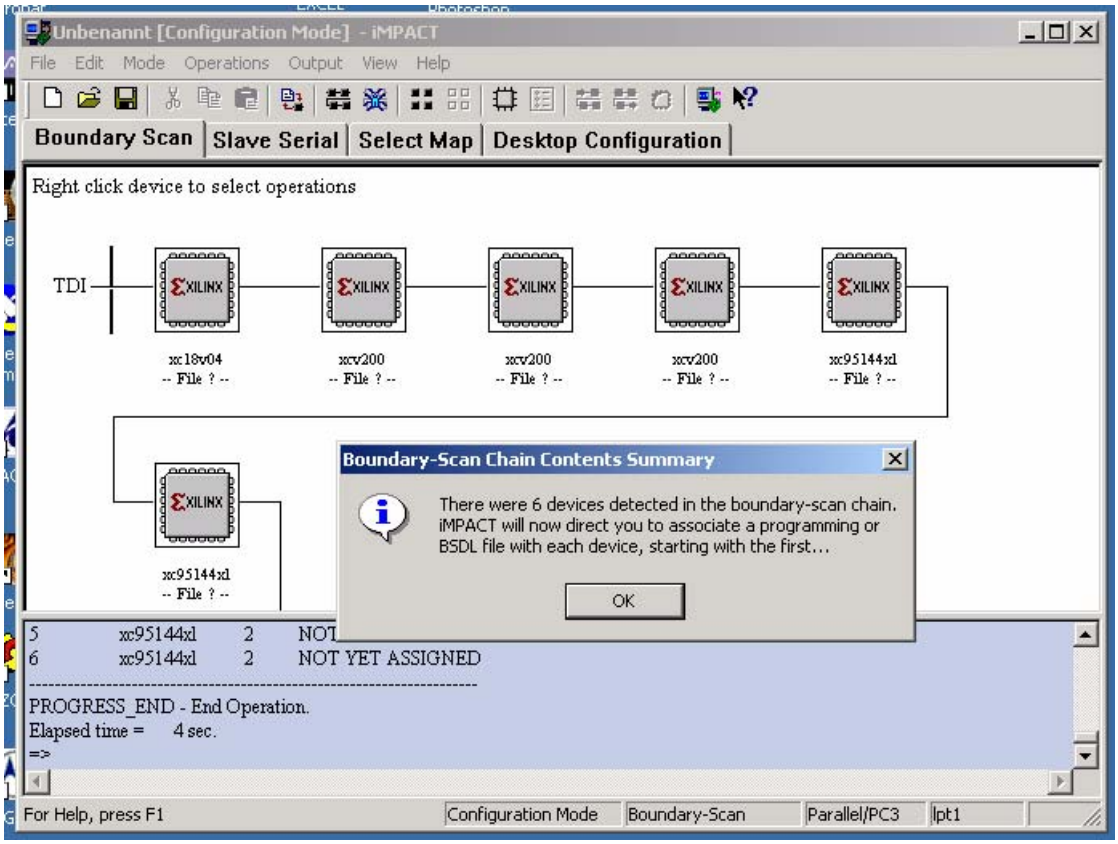
The JTAG chain will have the XC18V04 prom as only component in that case as shown below.



5 SIS3100 with SIS9200 DSP

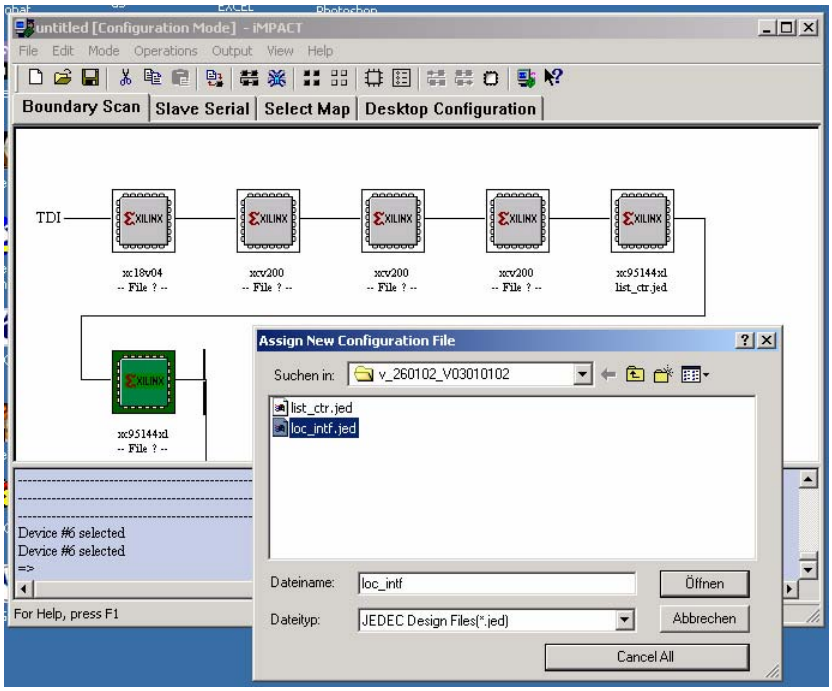
5.1 Initialize chain

With the SIS9200 installed you should see a total of 6 devices as illustrated below. The 2 additional devices are XC95144 EPLDs. Program the XC18V04 serial PROM as described in the DSP-less case first.



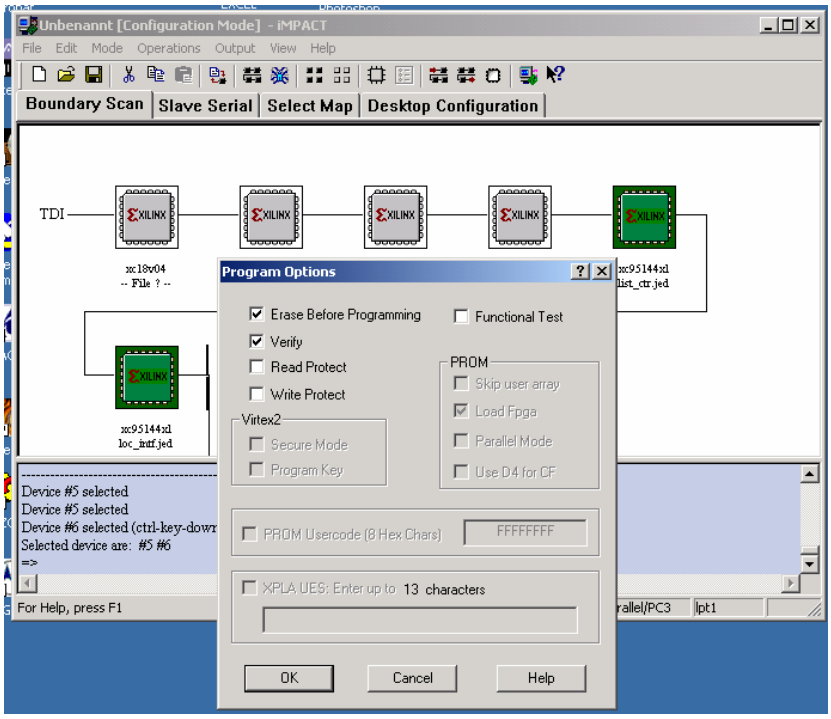
5.2 Select programming files

Select the programming files for the two EPLDs as described earlier. Device #5 (the first EPLD) will be loaded with the file list_ctr.jed, device #6 with loc_intf.jed.



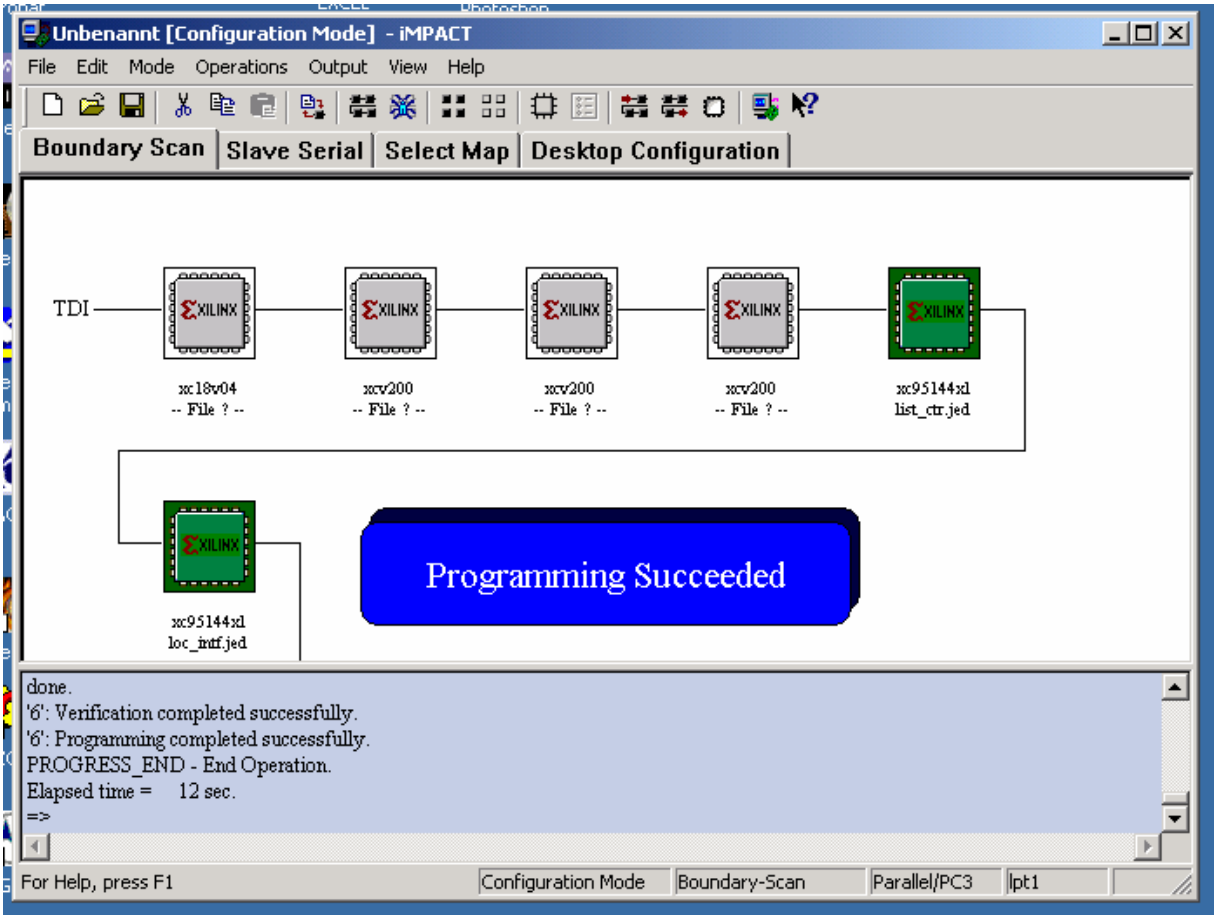
5.3 program EPLDs

You can select both EPLDs and program them in one go.



5.4 Completed

Upon successful completion you will see the programming succeeded popup for a moment.



6 SIS1100

The same steps as for the SIS3100 apply for the SIS1100. At shipment the combination of SIS1100-CMC and SIS1100-OPT is connected to give one JTAG chain.
Note: The SIS1100 has to be powered up for programming.

6.1 Initialize Chain

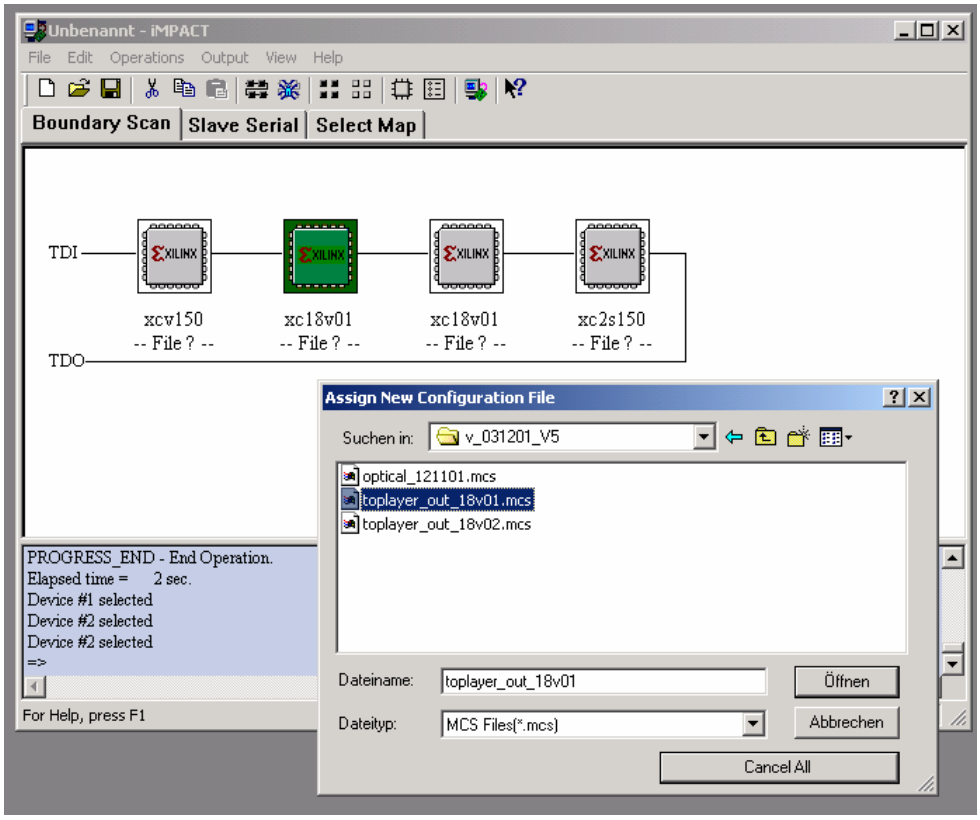
Four devices should be detected, 2 XCV150 or XC2S150 FPGAs and two XC18V01 or 02 serial proms. The chain should look like below. The left hand side serial PROM is on the SIS1100-CMC carrier card, the right hand serial PROM resides on the SIS1100-OPT Gigabit CMC card.

6.2 Select programming files

Depending on the upgrade one or two serial PROMS will be assigned a programming file, the FPGAs

1. define the file for the second device (toplayer_out_18v01.mcs) and the chip (xc18v01_vq44)
2. define the file for the third device (optical_121101.mcs) and the chip (xc18v01_vq44)

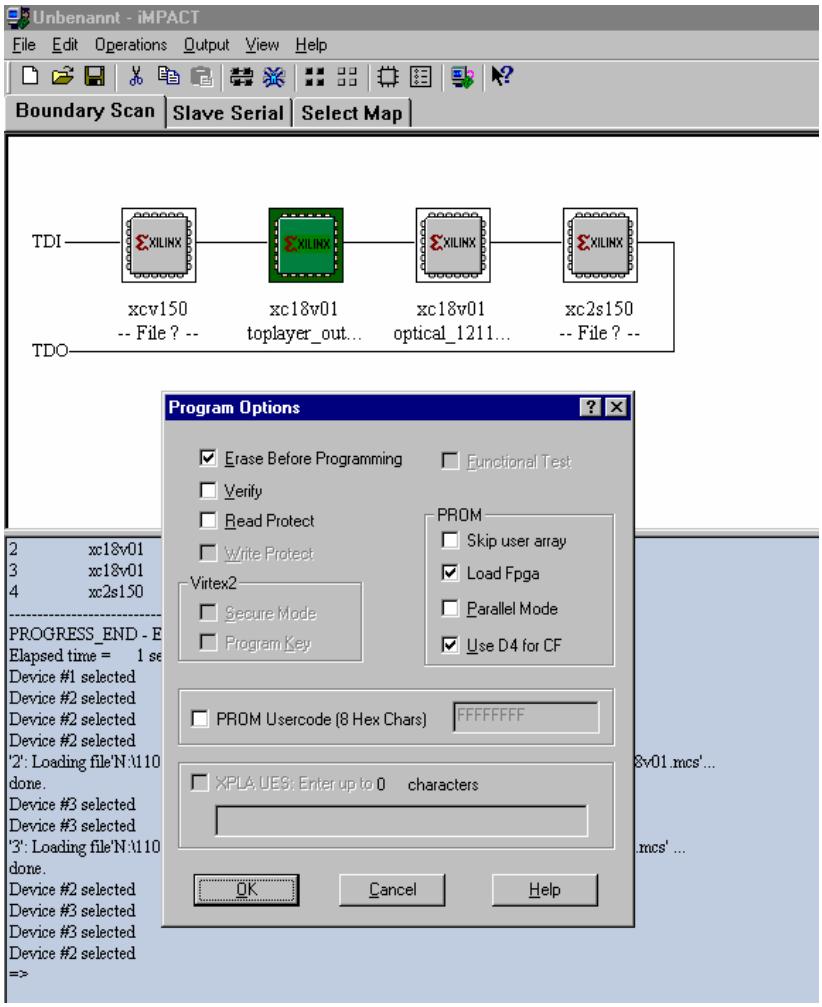
Note: CMCs from the first Juelich batch were stuffed with XC18V02 chips, the



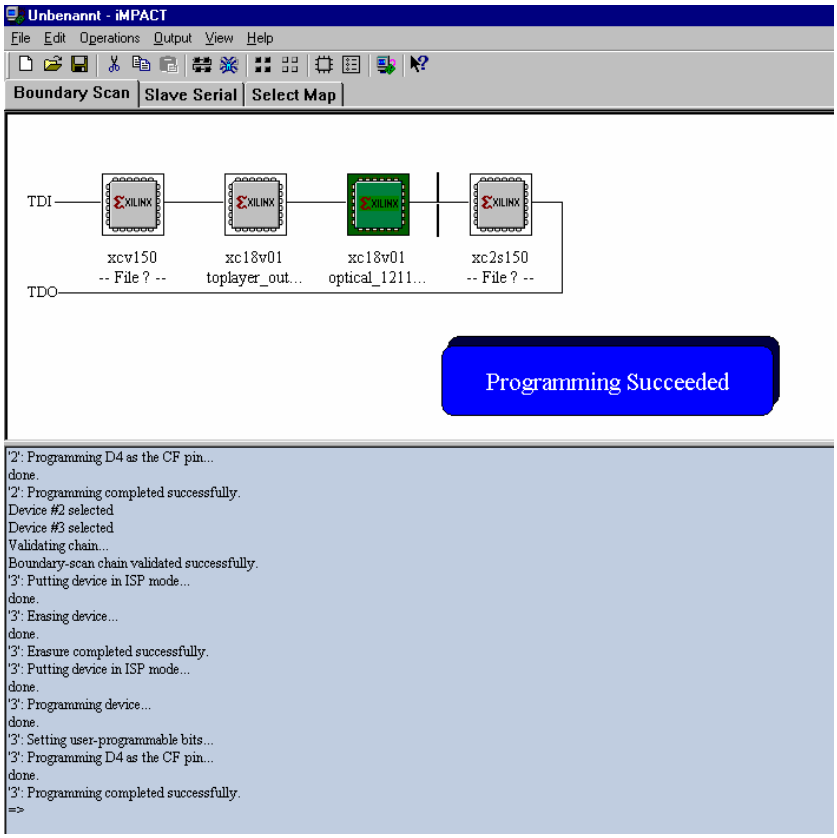
corresponding programming file has to be used in this case.

6.3 Program

1. click on the the second device (green) and then klick on Operation/Program and type OK



Do the same procedure for the third device.



7 SIS3820

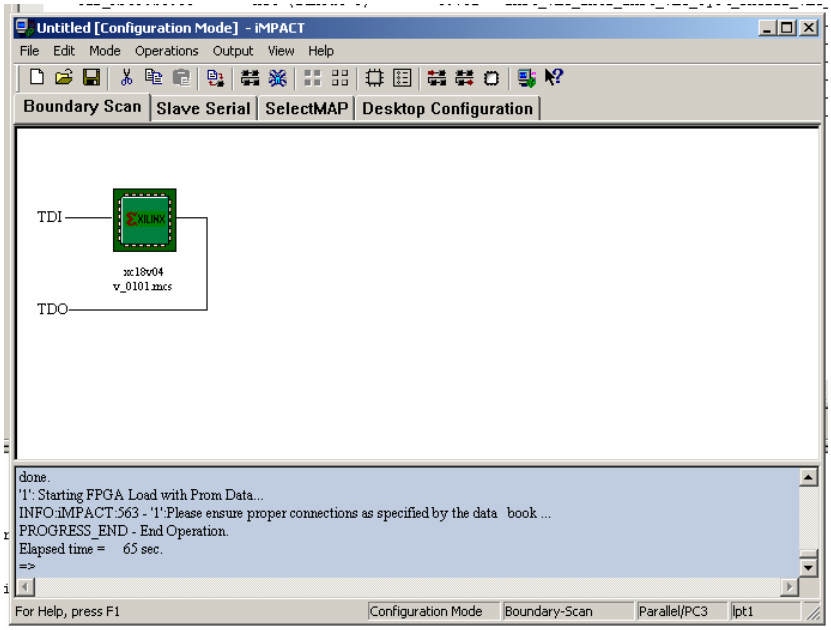
The SIS3820 family has the same name and pinout for the JTAG connector J500 as the SIS3100 board

7.1 watchdog disable

Close the lowest position of jumper J90 to disable the watchdog before upgrading the firmware.

7.2 JTAG chain

The SIS3820 has one serial PROM in the JTAG chain only.



7.3 Programming

Program the serial PROM in the same fashion as described for the SIS3100 earlier in this document

7.4 watchdog enable

Open the lowest position of jumper J90 to activate the watchdog after upgrading the firmware.

At this stage the new firmware should be rolled in on all cards and you can use the modules with the new firmware after a power down/power up cycle.