SIS3300
1105 Firmware - Greta

Addendum
to
User Manual
sis3300_greta_v111.doc

SIS GmbH
Harksheider Str. 102A
22399 Hamburg
Germany

Phone: ++49 (0) 40 60 87 305 0
Fax: ++49 (0) 40 60 87 305 20

email: info@struck.de
http://www.struck.de

Version: sis3300-M-1105-1-greta-addendum.doc as of 30.05.2011

Revision Table:

Revision	Date	Modification
1.00 Addendum	30.05.11	**Firmware Version: 1105** change Timestamp logic • Add new Timestamp Clear modes - clear with first stop trigger after each bank-switch (as before) - disable Timestamp clear - clear with first stop trigger after starting “auto bank switch mode” - clear with VME Write (Key Address) - clear external NIM Signal (LEMO In 1, User In) • expanded Timestamp-Counter width from 24 to 48 bit (max. Event Timestamp-Entries reduced from 1024 to 512) • add Timestamp Latch registers (bank switch)

1 Table of contents

2 Modifications/Add-Ons

2.1 Timestamp Clear modes

Two bits of the Control register are used to define the Timestamp Clear mode:
Timestamp Clear mode bit 1 and 0 (bit 13/12 to set; 29/28 to clear)

2.1.1 Control/Status Register(0x, write/read)

```
#define SIS3300_CONTROL_STATUS      0x0     /* read/write; D32 */
```

Bit	write Function	read Function
31	Clear reserved 15 (*)	
30	Clear reserved 14 (*)	
29	Clear Timestamp Clear mode bit 1 (*)	
28	Clear Timestamp Clear mode bit 0 (*)	
27	Clear reserved 11 (*)	
26	clear bank full pulse to output 3 (*)	
25	clear bank full pulse to output 2 (*)	
24	clear bank full pulse to output 1 (*)	
23	Clear reserved 7 (*)	
22	Disable internal trigger routing (*)	
21	Activate trigger upon armed (*)	
20	Non inverted trigger output (*)	
19	Don't use delay locked loop for external clock	Status P2_SAMPLE_IN
18	Enable user output/disable trigger output (*)	Status P2_RESET_IN
17	Clear user output (*)	Status P2_TEST_IN
16	Switch off user LED (*)	Status User Input
15	Set reserved 15	Status Control 15
14	Set reserved 14	Status Control 14
13	Set Timestamp Clear mode bit 1	Status Timestamp Clear mode bit 1
12	Set Timestamp Clear mode bit 0	Status Timestamp Clear mode bit 0
11	Set reserved 11	Status Control 11
10	set bank full pulse to output 3	Status Bank full pulse on LEMO output 3
9	set bank full pulse to output 2	Status Bank full pulse on LEMO output 2
8	set bank full pulse to output 1	Status Bank full pulse on LEMO output 1 (highest priority)
7	Set reserved 7	Status Control 7
6	Enable internal trigger routing	Status trigger routing (1= to input, 0=don't route)
5	Activate trigger upon armed and started	Status trigger generation (1=armed and started, 0=armed)
4	Invert trigger output	Status trigger output inversion(1=inverted, 0=straight)
3	Use delay locked loop for external clock (SIS3301 11 03 only)	Status delay locked loop for external clock
2	Enable trigger output/disable user output	Status of user/trigger output (1=trigger output, 0=user output)
1	Set user output (if bit 2 is not set)	Status User Output (1=output on, 0=output off)
0	Switch on user LED	Status User LED (1=LED on, 0=LED off)

(*) denotes power up default setting

Timestamp Clear mode bit setting table:

Timestamp Clear mode bit 1	Timestamp Clear mode bit 0	Timestamp-Counter Clear with
0	0	first stop trigger after each bank-switch (as before)
0	1	never
1	0	first stop trigger after starting “auto bank switch mode”
1	1	VME Write to Key-Address KEY_TIMESTAMP_CLR or External NIM signal (LEMO In 1, User In) (> 2 sample clocks)

2.1.2 Key address VME Timestamp Clear (0x38, write)

```
#define SIS3300_KEY_TIMESTAMP_CLR          0x38  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will clear the Timestamp Counter.

2.2 Timestamp Counter width expanded from 24 bit to 48 bit

The width of the Timestamp Counter is expanded from 24 to 48 bit.
As a result the function of the Event Timestamp Directory Entries have changed.
The max. number of Timestamp Entires is reduced from 1024 to 512.

2.2.1 Event Time Stamp directory bank 1 (0x1000-0x1ffc, read only)

```
#define SIS3300_EVENT_TIMESTAMP_DIR_BANK1    0x1000
                                    /* read only; D32, BLT32; size: 0x1000 */
```

offset address	Time Stamp (D23:D0)
0x0	Upper Time Stamp 0 (bits 47:24)
0x4	Lower Time Stamp 0 (bits 23:0)
0x8	Upper Time Stamp 1 (bits 47:24)
0xC	Lower Time Stamp 1 (bits 23:0)
..	
0xff8	Upper Time Stamp 511 (bits 47:24)
0xffc	Lower Time Stamp 511 (bits 23:0)

2.2.2 Event Time Stamp directory bank 2 (0x2000-0x2ffc, read only)

```
#define SIS3300_EVENT_TIMESTAMP_DIR_BANK2    0x2000
                                    /* read only; D32, BLT32; size: 0x1000 */
```

As for bank 1.

offset address	Time Stamp (D23:D0)
0x0	Upper Time Stamp 0 (bits 47:24)
0x4	Lower Time Stamp 0 (bits 23:0)
0x8	Upper Time Stamp 1 (bits 47:24)
0xC	Lower Time Stamp 1 (bits 23:0)
..	
0xff8	Upper Time Stamp 511 (bits 47:24)
0xffc	Lower Time Stamp 511 (bits 23:0)

2.3 Timestamp Latch registers

In Auto bank switch mode the timestamp counter will be latched into registers with a bank switch.
Four registers are implemented:

Offset	Size in Bytes	BLT	Access	Function
0x00000070	4	-	R	Upper Time Stamp Bank1 Latch (bits 47:24)
0x00000074	4	-	R	Lower Time Stamp Bank1 Latch (bits 23:0)
0x00000078	4	-	R	Upper Time Stamp Bank2 Latch (bits 47:24)
0x0000007C	4	-	R	Lower Time Stamp Bank2 Latch (bits 23:0)

The Time Stamp Bank1 Latch registers will be updated with the bank-switch from bank1 to bank2 (timestamp at the end of bank1).

The Time Stamp Bank2 Latch registers will be updated with the bank-switch from bank2 to bank1 (timestamp at the end of bank2).