struck innovative systeme

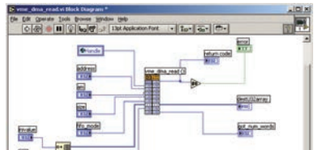
Board Level Electronics

SIS3153 USB3.0/Ethernet to VME Interface

The SIS3153 is the latest extension to our VME interface product line. It combines the ease of use and convenience of USB with transfer speeds known from our SIS110e/3104 optical interfaces to date only, as long as the maximum cable length is not a limitation for your application. Block transfer speeds in the order of 90 MByte/s are reached with the SFP GBit/s Ethernet option.

Functionality
- Single width 6U VME master/system controller
- USB3.0/Superspeed USB functionality
- 2 inputs/2outputs 00 LEMO, NIM/TTL level programmable
- SFP cage for copper or optical GBit/s Ethernet link
- all relevant VME addressing modes up to 2eSST
- performant single cycle list array execution

Software Support
- Windows, LINUX and OS X support
- Labwindows CVI/Labview/ROOT support
- SIS3150 compatible calls



Labview Example: Block Diagram of Block Read

SIS3153

SIS3316 16 Channel VME Digitizer Family
SIS3316-250-14 250 MS/s 14-bit or 125 MS/s 16-bit

With the SIS3316 board family we double the channel density to 16 synchronously sampling digitizer channels per single width VME card. Low power consumption dual ADC chips are used in combination with Xilinx Spartan 6 FPGAs. In addition to a performant VME slave interface a SFP cage allows for high speed point to point readout implementations like GBit/s Ethernet.

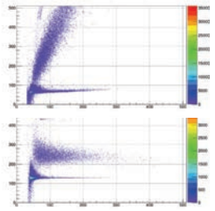
Functionality
- 16 channels
- 14/16-bit resolution
- 250/125 MSample/s per channel
- > 125/62.5 MHz analog bandwidth
- 128 MSample/channel memory
- Programmable offset DACs
- Two programmable gain settings
- 50 Ω /high impedance programmable
- Internal/external/external multiplied clock
- Random clock mode for slow acquisition
- Firmware discriminator (16 individual thresholds)
- Trigger input and output
- Coincidence trigger matrix
- Trigger bus
- Flexible acquisition and readout modes
- Readout in parallel to acquisition
- A32/D32/BLT32/MBLT64/2eSST
- Generic and application specific firmware designs
- LEMO 00 connectors (FBM on request)
- SFP socket for high speed link readout
- In field JTAG and VME firmware upgrade

SIS3316

SIS3316-DT 16 Channel Desktop Digitizer

SIS3316-DT

Standalone version based on SIS3316 VME card
- 19 - 36 V DC Power supply
- GBit/s Copper/Optical Ethernet readout



Onboard n/γ pulse shape discrimination illustration

photographs: struck innovative systeme
front page labview plot courtesy inl

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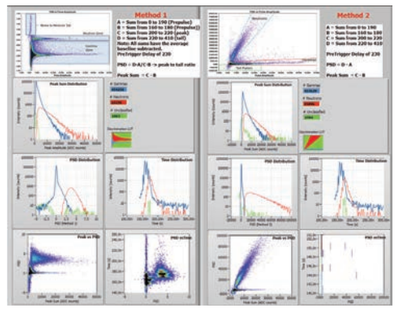
QUALITY SYSTEM CERTIFICATION DNV·GL ISO 9001

Welcome to the 2016 conference season. Several hundred of our MTCA.4 125 MSPS 16-bit SIS8300-x digitizers and associated RTMs are currently being installed at the European XFEL and the PAL FEL. Follow up developments are under discussion for the next accelerators, which are under construction.

On the non-MTCA digitizer side we cover up to dual channel 1.6 GSPS/single channel 3.2 GSPS 12-bit with our SIS1332 quad lane PCI Express card (see below). Our 16 channel SIS3316 VME digitizers (see last page) attract increased interest in detector readout, Plasma Physics and accelerator applications.



Our Product Range
- MTCA.4 Digitizers/Scalers/Digital I/O/RTMs
- VME Digitizers/ADCs
- VME Interfaces/Bus Couplers
- VME Scalers/Digital I/O
- PCI Express Digitizers
- Custom Designs

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SIS8300-L2 10 channel 16-bit 125 MS/s MTCA.4 Digitizer

The SIS8300-L2 is the current board of the SIS8300 digitizer family. It allows for more flexible configuration of the Zone 3 and the analog performance was further enhanced for LLRF operation im combination with the DWC8300 Downconverter RTM.

Functionality
- MTCA.4
- 4 lane PCI Express connectivity
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel sampling speed
- XC6VLX130T-2FFG1156C Xilinx
- Dual boot
- 2 GByte DDR3 memory
- AC or DC input stage
- ADC inputs through Rear Transition Module (RTM)
- internal, front panel, RTM and backplane clock sources
- Two 16-bit DACs for fast feedback implementation
- Front panel or Zone 3 DAC routing
- FPGA, RTM_CLK4, DIV0 and DIV1 DAC clock sources
- High precision clock distribution circuitry
- Programmable delay of dual channel digitizer groups
- Gigabit link port implementation to backplane
- 6.5 GBit/s on point to point links
- Extended MGT clocking scheme
- Twin SFP card cage for high speed system interconnects
- Front panel grounding block
- MMC 1.0 under DESY license LV91
- Zone 3 class A1.1 compatible (A1.0C and A1.1CO optional)

SIS8300-L2 MTCA.4 Digitizer

Note: A SIS8300-L2S version without DAC, front panel SMA and Harlink connectors is available also.

Related product: SIS8325 10-channel 16-bit 250 MS/s digitizer

SIS8300-L2/DWC8300 Data

(courtesy DESY)

DWC8300 MTCA.4 Downconverter RTM

The DWC8300 is a MTCA.4 downconverter RTM. It was developed at DESY for LLRF applications under the designation DRTM-DWC10 and is built by Struck under license of DESY.

Functionality
- MTCA.4 RTM implementation
- 10 Channels
- 8 Channel FBM multi coax. connector (CH1 to CH8)
- CH0 and CH9 SMA
- 700 MHz - 4 GHz
- Various intermediate frequencies
- Switchable front end attenuators
- LO clock from front panel or RF backplane
- LO power level monitor
- Digitizer clock input (5 - 130 MHz) from front panel or RF backplane
- I^2C support
- Zone 3 class A1.1 compatible

DWC8300 RTM

Production under DESY license LV 63

Production under DESY license LV 74

DS8VM1 Direct Sampling/Vectormodulator RTM

The DS8VM1 Downconverter/Vectormodulator RTM was developed at DESY for lower frequency single cavity LLRF applications under the designation DRTM-DS8VM1.

DS8VM1 RTM

Functionality
- MTCA.4 RTM
- 8 Channels DC or AC on FBM multi coax. connector
- DC - 400 MHz or 5 MHz – 700 MHz
- 2 Channels DC on MMCX connectors
- Switchable front end attenuators
- VM output 50MHz - 1 GHz
- Switchable output attenuator
- REF power level monitor
- Digitizer clock input (10 - 700 MHz) from front panel or RF backplane
- MMCX clock, interlock and sync. reset input
- On board clock generation/distribution
- I^2C support
- Zone 3 class A1.1 compatible

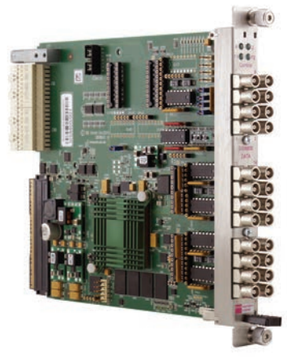
Production under DESY license LV 74

SIS8900 MTCA.4 Single Ended Input RTM

The SIS8900 RTM is used to feed single ended -50 Ω terminated- signals to the SIS8300 digitizer. Access to RTM _CLK0, RTM_CLK1 and RTM_CLK2 and a couple of digital I/O lines is implemented in addition.

Functionality
- MTCA.4 RTM
- 8-Bit I/O expander for I^2C-bus
- 10 LEMO 00 connectors (FBM option)
- 50 Ohm input impedance
- -1 V,...,+1 V default input range
- AC OR DC input configuration
- RJ45 jack for RTM clocks
- RJ45 jack for Digital I/O
- +5V, 250 mA power option for RJ45 jacks
- Two metric on board pin headers for 6 LVDS input/output signals each
- Zone 3 class A1.1 compatible

SIS8900 RTM



SIS8800 MTCA.4 Scaler

DWC8VM1 Downconverter/ Vectormodular RTM

The DWC8VM1 Downconverter/Vectormodulator RTM was developed at DESY for single cavity LLRF applications under the designation DRTM-DWC8VM1 and is built by Struck under license of DESY.

Functionality
- MTCA.4 RTM
- 8 Channels Downconverter on FBM multi coax. connector
- 2 Channels DC on MMCX connectors
- 500 MHz - 4 GHz (HF Version 5.7 GHz)
- Various intermediate frequencies
- Switchable front end attenuators
- VM output 50 MHz - 6 GHz
- Switchable output attenuator
- LO clock from front panel or RF backplane
- LO and REF power level monitor
- Digitizer clock input (5 - 130 MHz) from front panel or RF backplane
- MMCX clock and interlock input
- I^2C support
- Zone 3 class A1.1 compatible

DWC8VM1 RTM

Production under DESY license LV 71

SIS8800 MTCA.4 Scaler/Digital I/O

The SIS8800 is the MTCA.4 follow up to our SIS3820 VME multi purpose scaler. It can be used standalone or in combination with the upcoming SIS8980 discriminator RTM or custom digital I/O RTMs.

Functionality
- MTCA.4
- 4 lane PCI Express connectivity
- XC6VLX130T-2FFG1156C Xilinx
- Dual boot
- 2 GByte DDR3 memory
- 16 front inputs NIM or TTL/LEMO, TTL,ECL or LVDS/flat cable
- 4 control in-/4 control front outputs
- 42 LVDS I/Os to Zone 3
- two MGTs to Zone 3
- MMC 1.0 under DESY license LV91
- Zone 3 class D1.1 compatible